AF ZJW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Chad A. Cobbley et al.	§	
	§	Group Art Unit: 2811
Serial No.: 10/672,750	§	
	§	Examiner: Blum, David S.
Filed: September 25, 2003	§	
	§	
	§	
For: STACKED DIE MODULE AND TECHNIQUES FOR FORMING A STACKED DIE MODULE	§	Atty Docket: MICS:0078-1/FLE/MAN (01-0752.01)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

April 27, 2005 — Robert A. Manware
Date

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on February 23, 2005, and received by the Patent Office on February 28, 2005.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be necessary to advance prosecution of the present application, to Account No. 13-3092, Order No. 01-0752.01/FLE (MICS:0078-1).

05/03/2005 HVUONG1 00000074 133092 10672750
01 FC:1402 500.00 DA

1. **REAL PARTY IN INTEREST**

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application. The Assignee of the above-referenced application will be directly affected by the Board's decision in the pending appeal.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. **STATUS OF CLAIMS**

Claims 35, 37-39, 45, 47-49, 63 and 65-70 are currently pending, are currently under final rejection and, thus, are the subject of this appeal.

4. **STATUS OF AMENDMENTS**

Appellants have not submitted any amendments subsequent to the Final Office Action mailed on December 1, 2004, and therefore, there are no outstanding amendments to be considered by the Board.

5. **SUMMARY OF CLAIMED SUBJECT MATTER**

The present application relates generally to semiconductor processing and, more particularly to an integrated circuit comprising a die stack coupled to a substrate. In summary, independent claims 35, 45 and 63 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack of at least two semiconductor is functional." *See e.g.*, page 12, lines 10-12; page 17, line 13 – page 18, line 3. Independent claims 38, 48 and 66 each recite

an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack." *See e.g.*, Figs. 5C and 5D; page 14, line 9 – page 15, line 6. Independent claims 68, 69 and 70 each recite an integrated circuit comprising a stack coupled to a substrate wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack is successively thinner than the previous die." *See e.g.*, Figs 4B and 4C; page 10, line 21 – page 11, line 17. Further, claims 35, 38 and 68 each recite an integrated circuit comprising a die stack coupled to a substrate; "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature." *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. Based on the similarity in the recited subject matter, the rejections will be discussed in the Argument Section (7) of this Appeal Brief, in accordance with the claim groupings set forth in this paragraph.

With regard to the aspect of the invention set forth in independent claim 35, discussions of the recited features of claim 35 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the semiconductor die is coupled together by a first adhesive, the first adhesive being curable at a first temperature. *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. The integrated circuit further comprises a substrate (32, 44)

coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature. *See e.g.*, Figs 2 and 3; *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. Claim 35 further recites that each die in the stack of at least two semiconductor die is functional. *See e.g.*, page 12, lines 10-12; page 17, line 13 – page 18, line 3.

With regard to the aspect of the invention set forth in independent claim 38, discussions of the recited features of claim 38 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the semiconductor die is coupled together by a first adhesive, the first adhesive being curable at a first temperature. *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. The integrated circuit further comprises a substrate (32, 44) coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature. *See e.g.*, Figs 2 and 3; *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. Claim 38 further recites that the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack. *See e.g.*, Figs. 5C and 5D; page 14, line 9 – page 15, line 6.

With regard to the aspect of the invention set forth in independent claim 45, discussions of the recited features of claim 45 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a

stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate (32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 45 further recites that each die in the stack of at least two semiconductor die is functional. *See e.g.*, page 12, lines 10-12; page 17, line 13 – page 18, line 3.

With regard to the aspect of the invention set forth in independent claim 48, discussions of the recited features of claim 48 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate (32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 48 further recites that the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack. *See e.g.*, Figs. 5C and 5D; page 14, line 9 – page 15, line 6.

With regard to the aspect of the invention set forth in independent claim 63, discussions of the recited features of claim 63 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance

with the present invention relates to an integrated circuit. The integrated circuit comprises a substrate (32, 44). *See e.g.*, Figs. 2 and 3. The integrated circuit further comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate (32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 63 further recites that each die in the stack of at least two semiconductor die is functional. *See e.g.*, page 12, lines 10-12; page 17, line 13 – page 18, line 3.

With regard to the aspect of the invention set forth in independent claim 66, discussions of the recited features of claim 66 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a substrate (32, 44). *See e.g.*, Figs. 2 and 3. The integrated circuit further comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate (32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 66 further recites that the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack. *See e.g.*, Figs. 5C and 5D; page 14, line 9 – page 15, line 6.

With regard to the aspect of the invention set forth in independent claim 68, discussions of the recited features of claim 68 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a stack (e.g., 70, 80, 90). *See e.g.,* Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the semiconductor die is coupled together by a first adhesive, the first adhesive being curable at a first temperature. *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. The integrated circuit further comprises a substrate (32, 44) coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature. *See e.g.*, Figs 2 and 3; *See e.g.*, page 12, lines 6-19; page 17, lines 10-13. Claim 68 further recites that each die in the stack is successively thinner than the previous die." *See e.g.*, Figs 4B and 4C; page 10, line 21 – page 11, line 17.

With regard to the aspect of the invention set forth in independent claim 69, discussions of the recited features of claim 69 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a stack (e.g., 70, 80, 90). *See e.g.,* Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate

(32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 69 further recites that each die in the stack is successively thinner than the previous die." *See e.g.*, Figs 4B and 4C; page 10, line 21 – page 11, line 17.

With regard to the aspect of the invention set forth in independent claim 70, discussions of the recited features of claim 70 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to an integrated circuit. The integrated circuit comprises a substrate (32, 44). *See e.g.*, Figs. 2 and 3. The integrated circuit further comprises a stack (e.g., 70, 80, 90). *See e.g.*, Figs 5A-5D; page 13, line 21 – page 15, line 6. The stack comprises at least two semiconductor die (e.g., 34, 38, 40; 46, 50, 54; 72-76; 82-86; 92-96). *See e.g.*, Figs. 2, 3 and 5A-5D. Each of the die is coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate (32, 44). *See e.g.*, Figs 2 and 3; page 12, lines 10-12; page 13, lines 9-18; page 17, line 13 – page 18, line 3. Claim 70 further recites that each die in the stack is successively thinner than the previous die." *See e.g.*, Figs 4B and 4C; page 10, line 21 – page 11, line 17.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 35, 37-39, 45, 47-49, 63 and 65-67 under 35 U.S.C. § 103(a) as being unpatentable over Pai (U.S. Pat. No. 6,503,776) in view of Huang (U.S. Pat. No. 6,753,206).

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 68-70 under 35 U.S.C. § 103(a) as being unpatentable over Pai (U.S. Pat. No. 6,503,776) in view of Hakey (U.S. Pat. No. 6,627,477) or Moden (U.S. Pat. No. 6,512,303).

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Sections 102 and 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 35, 37-39, 45, 47-49, 63 and 65-70 are currently in condition for allowance.

A. Ground of Rejection No. 1:

The Examiner rejected claims 35, 37-39, 45, 47-49, 63 and 65-67 under 35 U.S.C. § 103(a) as being unpatentable over Pai et al. (US 6,503,776) in view of Huang (US 6,753,206). Appellants respectfully traverse this rejection. Each of the independent claims will be grouped and discussed below in accordance with subject matter commonly recited among each group, as summarized above in Section 5 of this Appeal Brief.

1. Judicial precedent has clearly established a legal standard for a prima facie anticipation rejection.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention

absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes all of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e.; something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

2. **The Examiner's rejection of independent claims 35, 45 and 63 is improper because the rejection fails to establish a prima facie case of obviousness.**

Independent claim 35 recites:

> An integrated circuit comprising:
> a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and
> a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two semiconductor die is functional.

Emphasis added.

Independent claim 45 recites:

> An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, *wherein each die in the stack of at least two semiconductor die is functional.*

Emphasis added.

Independent claim 63 recites:

> An integrate circuit package comprising:
> a substrate; and
> a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;
> *wherein each die in the stack of at least two semiconductor die is functional.*

Emphasis added.

The Examiner rejected independent claims 35, 45, and 63 under 35 U.S.C. § 103(a) as being unpatentable over Pai (U.S. Pat. No. 6,503,776) in view of Huang (U.S. Pat. No. 6,753,206). Appellants respectfully traverse this rejection. Specifically, Appellants respectfully submit that the cited references, taken alone or in combination, do not disclose or teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack of at least two semiconductor is functional."

Claims 35, 45 and 63 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die

in the stack of at least two semiconductor die is functional." In contrast, the Pai reference discloses a die stack where a part of the stack includes a "dummy chip" with film adhesive that adheres to other die within the stack. Col. 3, line 65 – Col.4, line 5. The dummy chip is a die similar to the other die in the stack, but the dummy chip does not include wiring "because it is not employed in the device operation." Col. 3, lines 20-22. In other words, the dummy chip in the stack disclosed in the Pai reference is non-functional. Accordingly, the Pai reference fails to teach or suggest a die stack wherein each of the die in the stack is functional as recited in the present claims.

In his rejection, the Examiner stated:

> Pai teaches a dummy die, the dummy die serving a function, thus being functional. The instant specification teaches that each die is tested to be functional, and in light of the specification, the Examiner believes that Pai reads on this limitation of being functional.

As discussed in the present specification, one of the disadvantages of prior stacking techniques is that damaged die may unknowingly be incorporated into a stacked package. Page 10, lines 7-9. In accordance with embodiments of the present invention, prior to attachment of the stack to a substrate, each of the die may be tested to ensure that all die in the stack are functional, thus forming a known good die stack (KGDS). Page 12, lines 10-12. The die stack can be electrically tested prior to attachment to a substrate. Page 17, lines 13-14. The die stack can be mechanically and structurally tested for functionality and/or reliability. Page 17, lines 15-16. Advantageously, functional testing can be used to screen die stacks before they are attached to a corresponding substrate. Page 17, lines 17-18. Faulty die stacks can be identified and scrapped prior to substrate attachment. Page 17, lines 18-19. Typical environmental and structural testing may include thermal cycling, temperature cycling, autoclave, vibration testing, etc. Page 17, lines 19-20. By assembling the die stacks

without prior attachment to a corresponding substrate, various reliability data can be gathered and failure mechanisms can be identified on the die stacks which may improve future design iterations, as well as prevent early failure of packages which have been incorporated into systems, such as the system 10. Page 17, line 20 – page 18, line 11. After desired testing, the die stacks may be attached to a substrate to form a package, such as those illustrated with reference to Figs. 2 and 3. Page 18, lines 1-3.

Appellants respectfully submit that in light of the present specification, it is clear that a "functional" die refers to an electrically functional die. Appellants further assert that those skilled in the art presented with the term "functional die" would certainly understand the term to refer to "electrically functional die." While the Examiner is correct in asserting that the dummy die of the Pai reference does indeed have a function, those skilled in the art would not interpret the dummy die disclosed in the Pai reference as a "functional die." Accordingly, Appellants respectfully submit that interpreting the dummy die of the Pai reference as "functional" simply because it does something or has a function is an unreasonably broad interpretation of the claim, since those skilled in the art would not make such a correlation.

Indeed, despite the Examiner's assertions regarding the functionality of the dummy die disclosed in the Pai reference, the Examiner goes on to cite the Huang reference and states that "Huang forms a stack similar to that of Pai, but teaches a stack where all die are 'electrically' functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang." While the Examiner asserted that the dummy die of the Pai reference is functional and thus that this limitation of the present claims is disclosed in the Pai reference, the Examiner then cites Huang as disclosing this particular limitation.

With regard to the Huang reference, Appellants respectfully submit that those skilled in the art would not be motivated to combine the Pai and Huang references, much less combine the references in the manner recited in the present claims. The Huang reference discloses a dual-chip integrated circuit package. "The dual-chip integrated circuit package includes a lead frame having a first set of leads and a second set of leads...in which the first integrated circuit chip is mounted on one side of the inner part of the first set of leads, and the second integrated circuit chip is mounted on the other side of the same..." Abstract. Accordingly, the Huang reference simply discloses coupling a first integrated circuit chip to the first side of a set of leads and coupling a second integrated circuit chip to the other side of a set of leads. As will be appreciated by those skilled in the art, lead frame technology is vastly different from technology related to packages incorporating a chip coupled to a substrate. Indeed, as discussed throughout the present specification, coupling a die or a die stack to a substrate may present certain challenges due to a mismatch in coefficients of thermal expansion of the die and the substrate. "The substrates on which the die are stacked generally have a different coefficient of thermal expansion." Page 3, lines 18-20. "Thus once the stack is formed on the substrate and cured as in typical die stacking systems, a mismatch in the coefficients of thermal expansion (CTEs) may be introduced, which may cause cracking or other problems with the die stack since the interface between each of the die and the interface between the die and the substrate are being cured at the same time but have different CTEs." Page 3, line 20 – page 4, line 1. Appellants provide this text as an example in support of the contention that those skilled in the art simply would not look to techniques for coupling die to lead frames as in the Huang reference, to modify integrated circuit packages where die are attached to substrates as in the Pai reference. Though the Huang reference does indeed illustrate a first functional die attached to one side of the lead

frame and a second functional die attached to a second side of the lead frame, there is absolutely no motivation from this reference to stack two functional die together and then attach them to a substrate in the manner recited in the present application.

Further, Appellants are unaware of how one skilled in the art could modify the package disclosed in the Pai reference in view of the Huang reference to achieve the recited integrated circuit package. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959); see M.P.E.P. § 2143.01. The Pai reference discusses perceived problems associated with multi-chip stacked packages including die attached directly to a substrate and stacked directly on top of each other. See background. To solve problems such as bond line thickness and CTE mismatch, the Pai reference teaches introducing a dummy die (i.e., a die which is not electrically functional) between functional die. Though Appellants do not know how one would modify the integrated circuit package of Pai in view of the integrated circuit package of Huang, assuming *arguendo* that such a modification could be made, this would destroy the principle of operation taught by the Pai reference. That is, the Pai reference explicitly teaches inserting a dummy die between functional die to create a consistent bond line. One skilled in the art would not be motivated to modify the Pai reference by removing the dummy die since it would destroy the principle of operation as taught by the Pai reference by reintroducing the inconsistent bond line thickness and the problems associated with CTE mismatch.

For at least the reasons set forth above, Appellants respectfully submit that claims 35, 45 and 63, as well as those claims dependent thereon, are not rendered obvious by the cited

combination. Thus, the Examiner's rejection of independent claims 35, 45 and 63, as well as those claims dependent thereon, is improper. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claims 35, 45 and 63, as well as those claims dependent thereon.

3. **The Examiner's rejection of independent claims 38, 48 and 66 is improper because the rejection fails to establish a prima facie case of obviousness.**

Independent claim 38 recites:

> An integrated circuit comprising:
> a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and
> a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;
> *wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.*
>
> Emphasis added.

Independent claim 48 recites:

> An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, *wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.*
>
> Emphasis added.

Independent claim 66 recites:

> An integrated circuit package comprising:
> a substrate; and
> a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

Emphasis added.

The Examiner rejected independent claims 38, 48, and 66 under 35 U.S.C. § 103(a) as being unpatentable over Pai (U.S. Pat. No. 6,503,776) in view of Huang (U.S. Pat. No. 6,753,206). Appellants respectfully traverse this rejection. Specifically, Appellants respectfully submit that the cited references, taken alone or in combination, do not disclose or teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack."

Claims 38, 48 and 66 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack." As described in the present specification, as amended, Figs. 5C and 5D are cross-sectional views of "shingle stacks." Page 14, line 10. Shingle stacks are die stacks wherein upper die may overhang die below them in the stack such that their centers are not aligned. Page 14, lines 11-12. Contrary to the Examiner's assertion, the Huang reference does not disclose a shingle stack as reasonable interpreted in light of the present specification. That is to say that the Huang reference does not disclose a die stack wherein an upper die overhangs a lower die. Even if the integrated circuit package disclosed in the Huang reference could be fairly characterized as a die stack, the upper die *does not* overhang the die below. The upper die does not "overhang" anything. As clearly illustrated in Fig. 2 of the Huang reference, the upper die is adhered directly and completely to a lead frame. Thus, no portion of the upper

die overhangs anything. Accordingly, neither of the cited references, either alone or in combination, discloses all of the features recited in claims 38, 48 and 66.

Because the cited references, taken alone or in combination, fail to disclose each of the features recited in claims 38, 48 and 66, Appellants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Further, as discussed in detail above with regard to the rejections of claims 35, 45 and 63, there is simply no suggestion to combine the cited references in the manner recited in the present claims. For this additional reason, Appellants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Thus, the Examiner's rejection of independent claims 38, 48 and 66, as well as those claims dependent thereon, is improper. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claims 35, 48 and 66, as well as those claims dependent thereon.

4. **The Examiner's rejection of independent claims 35 and 38 is improper because the rejection fails to establish a prima facie case of obviousness.**

In addition to the arguments set forth above, Appellants submit that the rejection of independent claims 35 and 38 is improper for an additional reason, as well. Claims 35 and 38 additionally recite an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claims 35 and 38, the Examiner stated:

> [i]t is noted that Pai teaches this (Col. 3, lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The Patentability of a product does not depend on its method of production. MPEP 2113.

While Appellants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Appellants respectfully traverse the Examiner's assertion that these claims are in fact product-by-process claims. As stated above, the claims recite a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." Emphasis added. The present claims do not recite an actual act of curing the adhesive. In contrast, the present claims recite physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Appellants respectfully submit that these structural limitations should indeed be given patentable weight.

Appellants respectfully submit that the Examiner's failure to give patentable weight to these structural limitations was improper. For this additional reason, Appellants respectfully

request that the Board overturn the Examiner's rejection and allow claims 35 and 38, as well as those claims dependent thereon.

B. **Ground of Rejection No. 2:**

1. **The Examiner's rejection of independent claims 68, 69 and 70 is improper because the rejection fails to establish a prima facie case of obviousness.**

Independent claim 68 recites:

> An integrated circuit comprising:
> a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and
> a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;
> *wherein each die in the stack of at least two die is successively thinner than the previous die.*
>
> Emphasis added.

Independent claim 69 recites:

> An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, *wherein each die in the stack of at least two semiconductor die is successively thinner than the previous die.*
>
> Emphasis added.

Independent claim 70 recites:

> An integrate circuit package comprising:
> a substrate; and
> a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;
> *wherein each die in the stack is successively thinner than the previous die.*

Emphasis added.

The Examiner rejected claims 68-70 under 35 U.S.C. § 103(a) as being unpatentable over Pai (US 6,503,776) in view of Hakey (US 6,627,477) or Moden (U.S. Pat. No. 6,512,303). Appellants respectfully traverse this rejection. Specifically, Appellants respectfully submit that the cited references, taken alone or in combination, do not disclose or teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die in the stack of at least two die is successively thinner than the previous die."

Claims 68, 69 and 70 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die in the stack of at least two die is successively thinner than the previous die." The Examiner cited the Pai reference in combination with either Hakey or Moden. The Hakey reference discloses a method of achieving coplanarity between chips. Col. 4, lines 62-63; Fig. 6. While it is true that the Hakey reference discloses chips 12 of the varying thicknesses in the Z-axis, these chips are attached directly to a substrate 10. See Fig. 3. That is to say, each of the chips 12 are positioned directly adjacent to one another, not on top of one another. Appellants respectfully submit that there is absolutely no motivation provided in either the Pai reference or the Hakey reference that would suggest using the die of varying thickness as provided in the direct mount package disclosed in the Hakey reference with the die stack of the Pai reference.

As repeatedly discussed throughout the Hakey reference, the reference is directed specifically to aligning the chips 12 adjacent to one another such that the active surface of the devices are co-planar. See e.g. Abstract; Fig. 6. Because the Hakey reference is directed to

ensuring that each of the active surfaces on the chips 12 are co-planar, the reference actually teaches away from forming a die stack. A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). In fact, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529 (Fed. Cir. 1988). Accordingly, it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145. The co-planar design of the Hakey reference cannot be maintained if the die are stacked. Because the Hakey reference actually teaches away from combining it with the Pai reference, the references cannot possibly be combined to render the recited subject matter obvious.

With regard to Moden, the Moden reference discloses a package comprising a semiconductor die 12 coupled to an adapter board 18 which is then coupled to a master board 30. Col. 4, lines 13-32. As explicitly stated in the Moden reference, the "adapter board" is a printed circuit board or substrate. Col. 3, lines 7-10. Appellants assume that the Examiner is applying the semiconductor die 12 and the adapter board 18 of the Moden reference to illustrate a die stack "wherein each die in the stack of at least 2 die is successively thinner than the previous die." However, it is clear that the Moden reference only discloses a package having a single semiconductor die 12. It is clear that the adapter board 18 disclosed in the Moden reference is *not* a semiconductor die. Therefore, the thickness of the adapter board 18 is irrelevant. The Moden reference does not disclose a stack of successively thinner die. For at least this reason, neither the Hakey reference nor the Moden reference, taken alone or in combination discloses each of the elements recited in claims 68, 69 and 70, much less provides any suggestion to combine these references in the manner recited in the present

claims. Accordingly, the cited combination cannot possibly render the recited subject matter obvious.

For at least the reasons set forth above, Appellants respectfully submit that claims 68-70, as well as those claims dependent thereon, are not rendered obvious by the cited combination. Thus, the Examiner's rejection of independent claims 68-70, as well as those claims dependent thereon, is improper. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claims 68-70, as well as those claims dependent thereon.

2. **The Examiner's rejection of independent claim 68 is improper because the rejection fails to establish a prima facie case of obviousness.**

In addition to the arguments set forth above, Appellants submit that the rejection of independent claim 68 is improper for an additional reason, as well. As with claims 35 and 38, claim 68 additionally recites an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claims 68, the Examiner stated:

> [i]t is noted that Pai teaches this (Col. 3, lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The Patentability of a product does not depend on its method of production. MPEP 2113.

As discussed above in Section 7. A.4 of this Appeal Brief, while Appellants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Appellants respectfully traverse the Examiner's assertion that these claims are in fact product-by-process claims. As stated above, the claims recite a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." Emphasis added. The present claims do not recite an actual act of curing the adhesive. In contrast, the present claims recite physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Appellants respectfully submit that these structural limitations should indeed be given patentable weight.

Appellants respectfully submit that the Examiner's failure to give patentable weight to these structural limitations was improper. For this additional reason, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claims 68, as well as those claims dependent thereon.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Appellants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Appellants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0078-1/FLE (01-0752.01).

Respectfully submitted,

Date: April 27, 2005

Robert A. Manware
Reg. No. 48,758
(281) 970-4545

8. **APPENDIX OF CLAIMS ON APPEAL**

Listing of Claims:

1-34. (Canceled)

35. An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two semiconductor die is functional.

36. (Canceled)

37. The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

38. An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

39. The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die.

40-44. (Canceled)

45. An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein each die in the stack of at least two semiconductor die is functional.

46. (Canceled)

47. The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

48. An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the

stack being coupled to a packaging substrate, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

49. The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die.

50-62. (Canceled)

63. An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein each die in the stack of at least two semiconductor die is functional.

64. (Canceled)

65. The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

66. An integrated circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

67. The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die.

68. An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two die is successively thinner than the previous die.

69. An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein each die in the stack of at least two semiconductor die is successively thinner than the previous die.

70. An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein each die in the stack is successively thinner than the previous die.